Novel CMOS Tunable Fuzzifier Circuit

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Abstract: A novel CMOS analog fuzzy membership function generator is designed. The fuzzifier generates the membership functions of a fuzzy system by converting the input analog signals to their corresponding predetermined grade of memberships. It takes voltage-mode inputs and produces current mode outputs and so it can be easily tuned with separate input voltages, for easy manipulations of the output fuzzy signals by the arithmetic operations that follow. Furthermore, the fuzzifier is so flexible that it can be readily adapted into most fuzzy systems, including neural networks, by changing the reference voltages and the number of building blocks used. The high speed of analog implementation also makes this fuzzifier more attractive than software approaches.
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1. Introduction

Fuzzy logic development has advanced in a fast pace in the past decade, and it has a wide range of applications. The major advantage of fuzzy logic is that it admits imprecision of data, thus, is able to model reality better than the traditional digital logic. In other words, traditional digital logic only describes black and white, while fuzzy logic describes the vast gray region in between black and white as well. In real life, situations are often described by linguistic terms. Fuzzy logic is capable to represent and process data given in these linguistic terms and generate results in these linguistic terms as well. Hence, fuzzy logic rules are more powerful in processing data. However, due to demand for higher speed and more compact hardware, analog VLSI is becoming more and more important in realization of fuzzy logic technologies. Hence, in this paper, we propose to develop an analog to fuzzy signal converter (fuzzifier) as a solution to convert ordinary analog signals into fuzzy signal in an efficient manner. It has the advantage of higher speed than the current software

2. Fuzzifier Block Diagram

As fuzzifier needs s-shape and z-shape membership functions, so to crate those functions two transconductor circuits are used, whichever to generate one of the z-shape or s-shape MFG's. Transconductor circuit is designed in a way that its slops and basis can be tuned easily with input control voltages. The block diagram of fuzzifierand working manner of it, are shown in Fig. 1.

As seen in Fig. 1 to generate trapezoidal membership functions a normal current is used and all three currents applied to minimum current selector block.

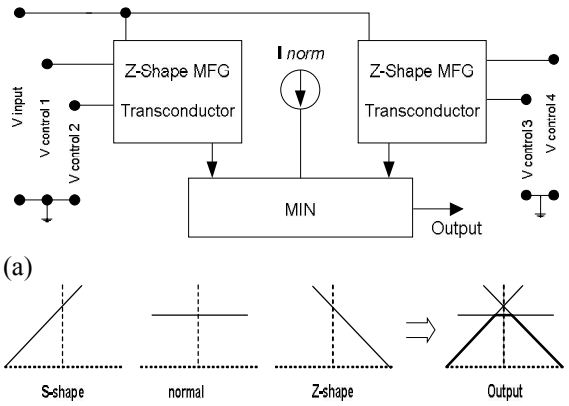


Fig. 1: (a) block diagram of fuzzifier circuit (b) working manner of fuzzifier circuit

3. Basic Circuit and the Transconductor

Fig. 2 shows a class-AB non-linear differential-input transconductor, which for $V_{CD} \geq \sqrt{I_B/\beta_1}$, has an output current defined by:

$$I_{OUT} = \beta_2 \left(V_{CD} + V_{eff1}\right)^2 \qquad (1)$$

Where $\beta_1 = 0.5\mu c_{ox}(W/L)$ is a MOSFET's transconductance parameter and $V_{eff1} = \sqrt{I_\beta/\beta_1}$ is an effective voltage of M1.

From the circuit arrangement, it can be seen that the circuit can be operated under $V_{sg} + 2V_{eff}$ supply voltage, which is compatible to low-voltage application.

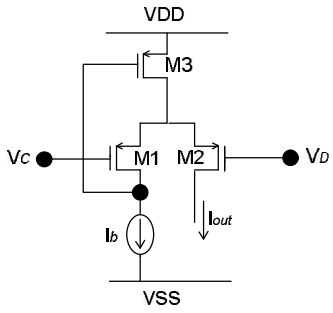


Fig. 2: Square-law differential-input transconductor

Fig. 3 shows the class AB linear transconductor realized by cross-coupling a pair of non-linear transconductors of Fig. 1 Assuming that M1-M4 are of identical dimensions, it can be found that for $|V_{AB}| \le \sqrt{I_A/\beta}$, the differential output current is linearly dependent on the differential input voltage,

$$I_{out} = I_{o1} - I_{o2} = \beta(V_{AB} + V_{eff1})^2 - \beta(V_{BA} + V_{eff1})^2 = 4V_{AB}\sqrt{I_A\beta_A} \quad (2)$$

Where $\beta_A = \beta_1 = \beta_2 = \beta_3 = \beta_4$. According to (2), it is clearly seen that the transconductance gain is a square-root function of the bias current I_A .

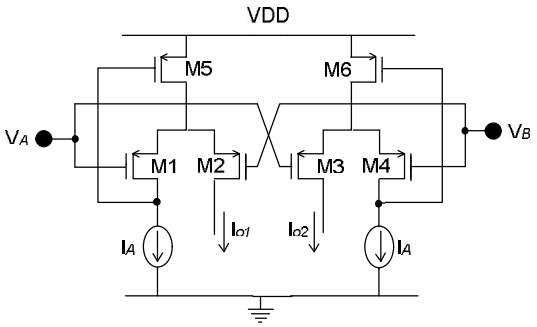


Fig. 3: Fully differential class-AB transconductor

Fig. 4 shows the proposed class-AB transconductor which utilizes the transconductor of Fig. 2 and 3 as the tuning circuit and the main voltage to current converter, respectively.

Referring to the transconductor in Fig. 4 current mirror Mb2-Mb4 is used to reflect the output current of the tuning circuit for biasing the main transconductor. If the dimensions of M7-M8 are identical, it can be shown that:

$$I_o = \beta_\beta\left(V_{CD} + \sqrt{\frac{I_\beta}{\beta_\beta}}\right)^2 \quad (3)$$

Where $\beta_B = \beta_7 = \beta_8$. Substituting (3) into (2) and rearrange the result, we have

$$I_{out} = 4V_{AB}\sqrt{\beta\left[V_{CD} + \sqrt{\frac{I_D}{\beta}}\right]^2\beta} = 4V_{AB}\beta\left[V_{CD} + V_{eff}\right] \quad (4)$$

According to (4), we found that the value of I_{out} is linearly dependent upon the sum of the controlled voltage V_{CD} and the square-root of I_B/β_β .

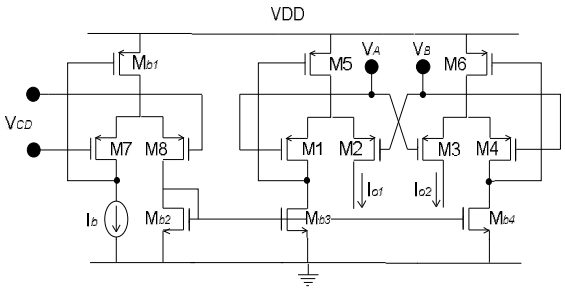


Fig. 4: Fully differential class-AB transconductor with tunable slop

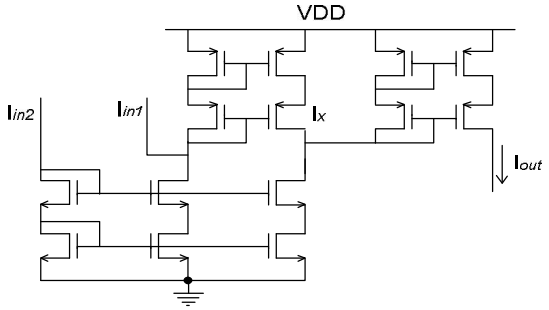


Fig. 5: Circuit diagram of the minimum current selector.

2. Minimum Current Selector

Circuit diagram of the used minimum current selector is shown in fig. 5. This block takes two sourcing currents and sources an output current which is equal to minimum of the inputs. The functionality of the circuit is simple and straightforward. If *Iin2* > *Iin1*, then the difference current of *Iin2* – *Iin1* in the input subtraction node flows in PMOS current mirror and then subtracted from *Iin2* in output subtraction node, resulting in:
Iout = *I in2* − (*I in2* − *I in1*) = *I in1*.

On the other hand, if *Iin1* > *Iin2*, then there is no difference current flowing in PMOS current mirror; hence in output subtraction node we have:
Iout = *I in2* − 0 = *I in2*.

As we see, the output current of the circuit is the minimum of two input currents.

The entire circuit of fuzzifier is shown in Fig. 6.

2. Simulation Results

The proposed fuzzifier has been simulated using Hspice and level 49 BSIM3V3 parameters. The circuit operates with a single supply voltage of 3.3V in a 0.35 µm CMOS technology.

Fig. 8 illustrates a simulated relationship between the differential output current and transconductance differential input voltage V_{AB}.

2. Layout of Circuit

The layout of the fuzzifier is shown in Fig. 7.The complete layout occupies an area of 38.9µm by 21.5µm.

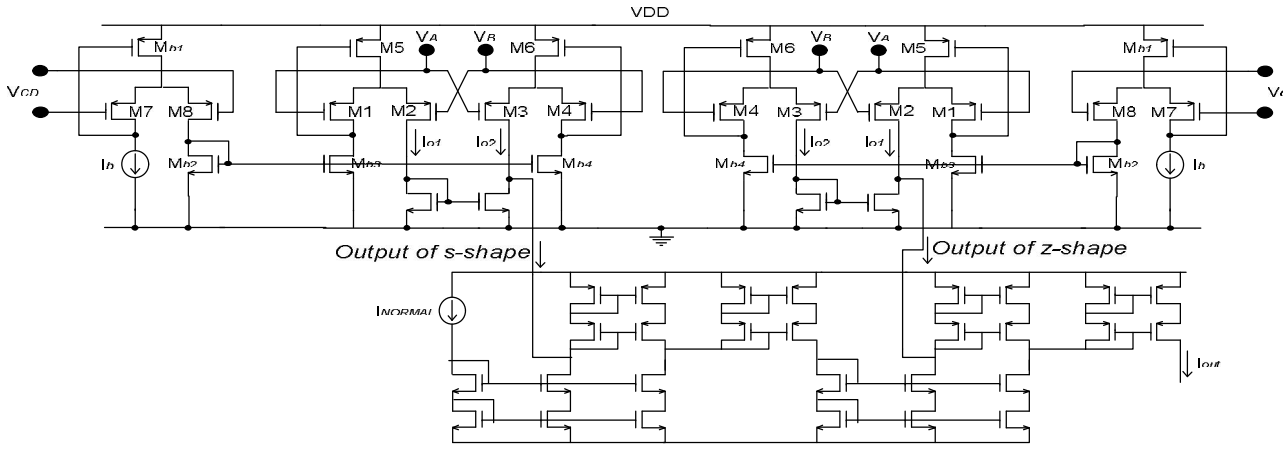


Fig. 6: The entire circuit of fuzzifier

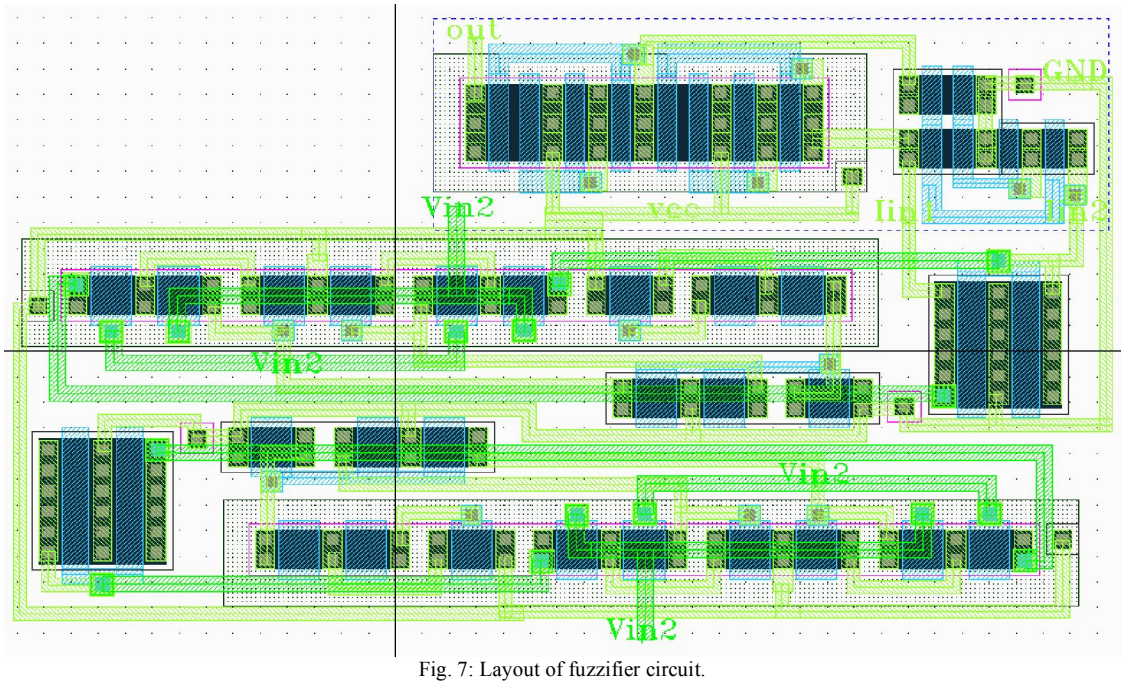


Fig. 7: Layout of fuzzifier circuit.

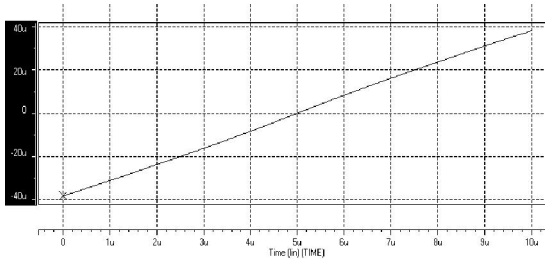
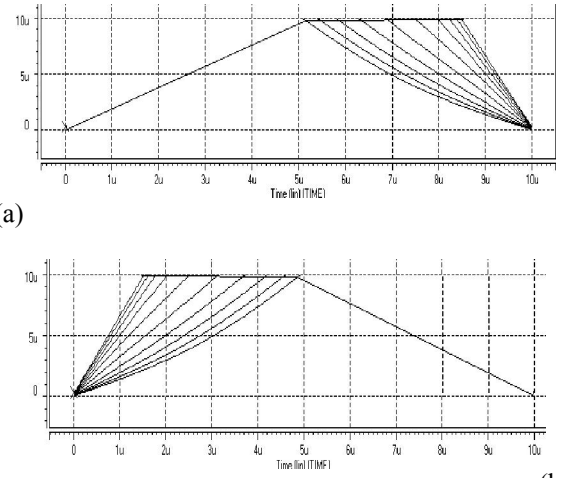


Fig. 8: The simulation result of transconductance

The simulation results of the membership function generator circuit for z-shape memberships with variable slops are shown in Fig. 9(a) and for s-shape memberships in Fig. 9(b). The input control voltage V_B (bases control voltage) is constant and the input control voltage V_{DC} (slops control voltage) is fixed in different value from 0-1.5 while $2V_{P-P}$ is applied to V_A input voltage.



(a)

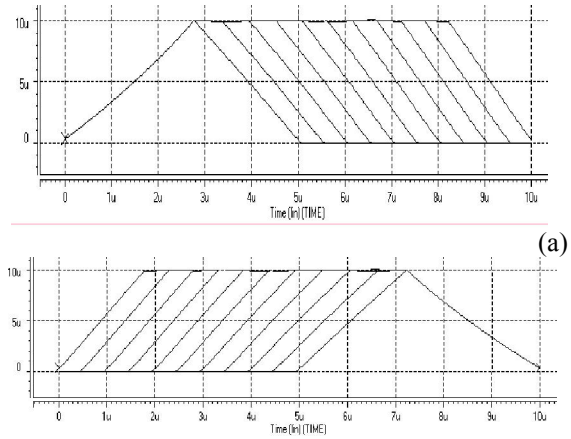
(b)

Fig. 9: The simulation result of fuzzifier with variable slop in (a) s-shape (b) z-shape membership functions

And the simulation results z-shape memberships with variable bases are shown in Fig. 10(a) and for s-shape memberships in Fig. 10(b). The input control voltage V_B (bases control voltage) is fixed in different value from 0.5-1.5 and the input control voltage V_{DC} (slops control voltage) is constant while $2V_{P-P}$ is applied to V_A input voltage.

Conclusions

A new CMOS voltage-input current-output fuzzy membership function has been presented. The fuzzyfier has input control voltages to tune the slops and bases of membership functions. The performances have been demonstrated using HSPICE simulations.



(a)

(b)

Fig. 10: The simulation result of fuzzifier with variable bases in (a) s-shape (b) z-shape membership functions

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